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Design and Simulation of Multirate Filter using BFD Multiplier Architecture

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Abstract: Interpolation and Decimation is very much effective in Multirate signal processing application. This paper proposes VLSI architecture polyphase decimation filter with decimation factor using BFD multiplier. High speed, area and power efficient are the main concerns in this VLSI design. The power dissipation can be reduced in polyphase decimation filter when uses with BFD multiplier which consumes low-power when compared to the conventional multiplier. The speed can be improved by using carry look ahead adder. This architecture also provides significant reduction in area (in terms of number of slices).

Keywords: Area, BFD multiplier architecture, Carry look ahead adder, Polyphase decimation filter, power dissipation, Speed.

I. INTRODUCTION

Polyphase decomposition is the vital techniques which plays an important role in Multirate signal processing. Polyphase structure utilize fir filter that leads to very efficient implementation. Less area and minimum power consumption are some of the most important factor for the DSP systems and high performance systems. the performance of a system is contributed by the performance of the multiplier. Power dissipation is the factor that changes speedily and is one of the major issues today. Text as instruments are making a digital circuit that does not require power supply. the power dissipation is minimizing by reducing the switching activity factor and by reducing number of operations to be in custody of filter structure. switching activity is reduce by adder and counter. the BFD multipliers have slightly less area and power than optimize tree multipliers while keeping similar delay. the reduction of power consumption is obtain via altering multiplicands in software without any hardware. spst (spurious Power Suppression Technique) is apply on multipliers for high-Speed and low power purposes.
A low power structure bypass zero, feed A directly (BZ-FAD) for shift and add multiplier architecture considerably minimize the switching activity. In this paper, FIR filter with power efficient BFD multiplier is preferred here to get reduction in power dissipation. This paper describe the design of polyphase filter with high speed, low power BFD multiplier architecture which use carry look ahead adder. This provide reduction in power dissipation as well as increase in speed when compare to conventional multiplier.

II. PROPOSED FILTER STRUCTURE

A filter can be realized with several ways such as cascade form, direct form. If the transfer function of the filter is decomposed into number of sub twigs then process is called polyphase realization.

A) Polyphase FIR Filter
FIR filter is a zero-phase filter. It has magnitude equal to unity in the pass band and zero in the stop band.FIR system is described by the difference equation shown in

$$y(n)\sum_{k=0}^{M-1} b_k x(n-k) \qquad (1)$$

Where filter coefficients y(n) & x(n) are output and input sequences. The equivalent system function is known in "(2)".

$$H(z) = \frac{Y(z)}{X(z)} = \sum_{k=0}^{M} b_k z^{-k} \qquad (2)$$

A linear-phase FIR filter of order N is characterized by symmetric impulse response given in "(3)".

$$h(n)=h(n-N) \qquad (3)$$

and asymmetric impulse response is given in "(4)"

$$h(n)=-h(n-N) \qquad (4)$$

In a general case, L-branch polyphase decomposition having transfer function of order N is given by "(5)".

$$H(z)\sum_{m=0}^{L-1} z^{-m} E_m z^{L} \qquad (5)$$

$$E_m = \sum_{n=0}^{\frac{n+1}{L}} h(n+m)\, z^{-m},\ 0 \le m \le -1$$

FIR filter is realized based on polyphase decomposition which leads a parallel structure. To point up this approach, a casual FIR transfer function H(z) of length nine is gives in "(6)"

$$H(z)=h(0)+h(1)z^{-1} + h(2)z^{-2}+.....+h(8)z^{-8} \quad (6)$$

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Which is a function of filter coefficients h(k),$0 \le k \le 8$.
The transfer function contain odd indexed coefficients and even indexed coefficients which is given by

$$H(z)=h(0)+h(2)z^{-2}+h(4)z^{-4}+h(6)z^{-6}+h(8)z^{-8}+z^{-1}[h(1)+h(3)z^{-2}+h(5)z^{-4}+h(7)z^{-6}$$

If grouping the same equation differently then

$$H(z)=E_0(z^3)+z^{-1}E_1(z^3)+z^{-2}E_2(z^3) \quad (7)$$

Equation (7) is represented in fig.1. The structure consist multipliers, delays and accumulators.

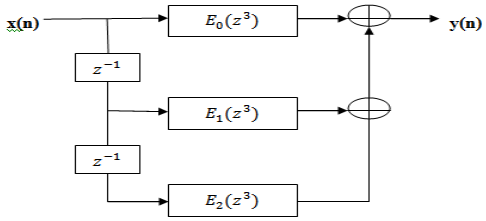

Fig.1 Polyphase FIR Filter Structure

B) Transposed Polyphase Decimation Filter
Decimation factor D is a positive integer develop an output sequence y(n) with a sampling rate is $(1/D)^{th}$ of the input sequence x(n). It is implemented by keeping each D^{th} sample of the input sequence and delete D-1 samples between successive samples. As a result, all input samples with indices, exact to an integer multiple of D and all others are discarded. The output sequence is generated according to the relation given in "(8)".

$$y(n)= x(nD) \quad (8)$$

The result is aliasing, to avoid the aliasing effect anti-aliasing filter called low pass filter can be use before down sampling. The transposed form of the decimation filter is used in this paper to let alone the shift registers used in tapped delay structure. X(n) comes into filter at the sample rate and is applied to all tap multipliers at the same time. The number of stages in the filter depends on the number of coefficients and value of decimation factor. The number of stages are exact to the number of coefficients divided by decimation factor. If coefficients are not a multiple of decimation factor then we have to add zeros.
The transpose form of polyphase filter for decimation factor of three is in fig.2. In this structure, in each cycle, input x(n) is pass through the tap multiplier. At the start input sequence x(n) is specified through a parallel input serial output shift register.
The output of PISO is fed to three sub-filter section at which the input sequences are processed in parallel form with serial input parallel output (SIPO) shift register. In each section, the input is multiplied with the coefficients. Since the processing is done in parallel so structure improves the speed of operation. When coefficient is multiply with the sample then coefficients and input samples are change during each cycle. The function of the accumulator is to mount up the value of multiplier for every 3(D) cycle. Carry look ahead adder is used to perform addition in order to rise the speed of system. The decimated output y(n) is obtain using this polyphase decimation filter.

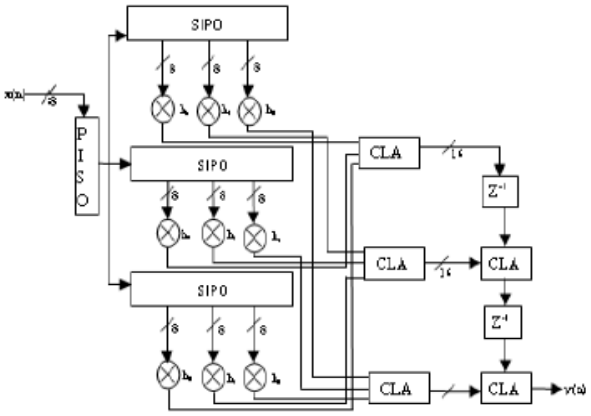

Fig.2. Transposed Filter structure

III. MULTIPLIER ARCHITECTURES

There are several multiplier to perform multiplications. Shift and add, booth multiplication, modified booth multiplication and spurious power control are some of the methods used to perform multiplication. In this paper BFD multiplier is compared with the conventional multiplier.

A. Conventional Multiplier:
In conventional multiplier, dynamic power dissipation is more because of switching activity during multiplication. There are six major sources of switching activity in conventional multiplier. These sources are:

(1) Shifting register content,
(2) Adder activity,
(3) Counter activity,
(4) A and 0 switching between the multiplexer,
(5) Multiplexer select activity,
(6) Partial product shifting.

B. BFD Multiplier
To reduce dynamic power dissipation, the switching activity must be reduce. The switching activity is reduced after changing some of the components and adding a bypass and feeder logic. Fig.3 shows the architecture of BFD multiplier where Y and X are the inputs. In the conventional shift and add multiplier, input is shifted which leads to some switching activity.

This is overcome by using one-hot encoded bus selector in BFD multiplier architecture, in each cycle. Counter is used to select Y(n) in the n^{th} cycle. In conventional shift and add multiplier, the present partial product is added to input X which gives needless transitions in the adder when Y(0) is zero. In this BFD multiplier architecture, the adder is bypass and the partial product should be shifted to the right by one bit. This minimizes unnecessary switching activities in the adder.

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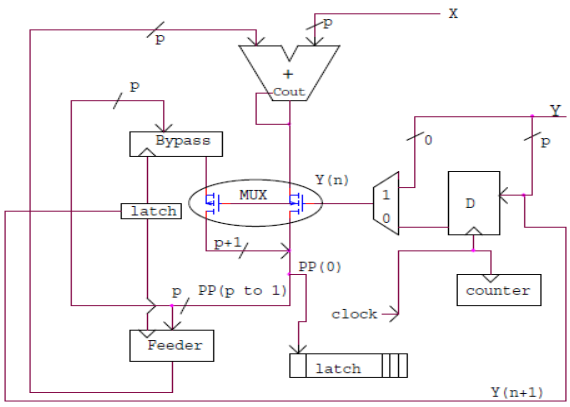

Fig.3 Architecture Of BFD Multiplier

In BFD multiplier architecture, in each cycle, the hot bit of the next cycle (Y(n+1)) is checked. If Y(n+1)= 0 then adder is not essential for the next clock cycle, to store the current partial product, the bypass register is clocked. If Y(n+1) is 1, the feeder register is clocked and this result should be fed to the adder in the next clock cycle. In the conventional shift and add architecture, the partial product is shifted in each cycle leads to transitions. During the first cycle, the least significant bit PP(0) of the product becomes analyzed and is stored in the right-most latch. In the subsequent cycles, the next least significant bits are analyzed and stored in the proper latches. When the last bit is stored in left-most latch, the higher and lower half of the partial product form the final product result. Comparing the two architectures, BFD multiplier saves power. Since, the lower half of the partial product is not shifted and this partial product is generated with latches instead of flip-flops. Since latch is a level sensitive device and flip-flop is an edge triggered device. In the conventional shift and add multiplier architecture, the transparent mode of latches prevents us from using latches instead of flip-flops for formation of lower half of the partial product. This problem does not exist in BFD multiplier since the lower half is not form by shifting the bits in a shift register.

The switching activity is reduced noticeably due to the shift of Y register, operations of the right input of the adder, multiplexer select line, counter operations, shifts in the partial product registers. In each cycle, If the hot bit Y(n) is zero, then there is no transition in the adder since the adder inputs do not change. Because in the past cycle, the partial product is stored in the bypass register and value of the feeder register, which is the input of the adder, remains unchanged. X is another input of adder which is held constant during the multiplication. This allows us to remove the multiplexer and feed input X directly to the adder.

This results in a noticeable power saving. Ripple carry adder is use in BFD multiplier. In this work, we are using carry look ahead adder . A carry look ahead adder is one of the fast adders used in digital logic circuits. It improves the speed by reducing the amount of time required to find out the carry bits. This adder calculates carry bits simultaneously before the sum, which reduces the waiting time to calculate the result of the larger value bits.

Conventional Multiplier	BFD Multiplier
1101 (13)	1101 (13)
× 1010 (10)	× 1010 (10)
0000	11010
+ 11010	+ 1101000
+	000000
+ 1101000	10000010 (130)
10000010 (130)	

Fig.4 Comparison between Multipliers

IV. PROPOSED PLAN

The basic purpose of design of Multirate filter using BFD multiplier is to reduce power consumption, speed and area of Multirate filter. The following flow chart shows propose plan of work. The design of Multirate filter is carried out according to the following steps:

- Study conventional multiplier
- Design BFD multiplier
- Design polyphase decimation filter
- Design Multirate filter
- Observe power, speed and area

V. SYNTHESIS AND SIMULATION RESULTS

A) RTL View of Multirate Filter

In this Multirate filter, there are four input sequences of 8 bit is applied along with the four impulse response having length 16 bit of each and at the input side one clock cycle is also given as an input. The output is of 16 bit each which partitioned into four part.

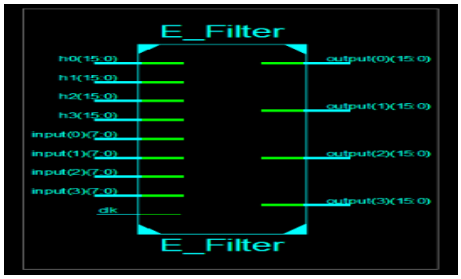

Fig.3. RTL View of Multirate Filter

B) Design Summary And Comparative Analysis Between Conventional And BFD Multiplier

Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slices	214	768	27%
Number of Slice Flip Flops	99	1536	6%
Number of 4 input LUTs	408	1536	26%
Number of bonded IOBs	66	97	68%
Number of GCLKs	1	8	12%

Fig.4 Conventional Multiplier

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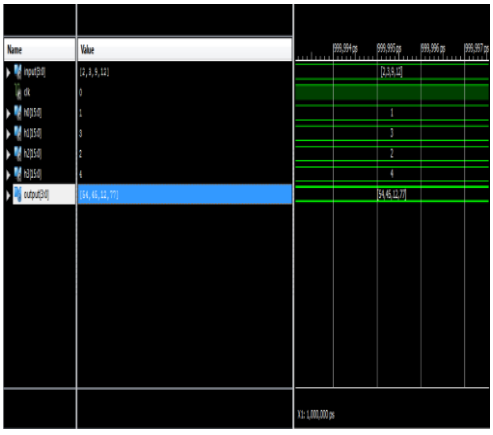
Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slices	141	768	18%
Number of Slice Flip Flops	99	1536	6%
Number of 4 input LUTs	271	1536	17%
Number of bonded IOBs	66	97	68%
Number of GCLKs	1	8	12%

Detailed Reports

Fig.5 BFD Multiplier

C) Simulation Result of Filter



D) Time Analysis Between Conventional And BFD Multiplier

Conventional Multiplier

```
All values displayed in nanoseconds (ns)

=========================================================
Timing constraint: Default path analysis
  Total number of paths / destination ports: 75334 / 16
---------------------------------------------------------
Delay:               21.143ns (Levels of Logic = 21)
  Source:            a<2> (PAD)
  Destination:       sum<15> (PAD)
```

BFD Multiplier

```
All values displayed in nanoseconds (ns)

=========================================================
Timing constraint: Default period analysis for Clock 'clk'
  Clock period: 9.310ns (frequency: 107.416MHz)
  Total number of paths / destination ports: 8001 / 159
---------------------------------------------------------
Delay:               9.310ns (Levels of Logic = 6)
```

VI. CONCLUSION

Polyphase decimation filter with area, high speed and power efficient BFD multiplier architecture has been propose in this paper. The proposed multirate filter design using BFD multiplier architecture exhibits a low power consumption in comparison to conventional multiplier architectures. The BFD multiplier reduced switching activity and in turn lead to reduced power consumption. The power dissipation and speed will be further improved by lowering switching activity and applying pipelining technique. The design can be verified using Xilinx software with VHDL code and power consumption will be analyzed using Xilinx xpower analyzer tool.

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BIOGRAPHIES

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